

April 15, 2004

To: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. $10/810,965 \quad 03/26/04$

Yen-Ming Chen et al.

NOVEL METHOD TO IMPROVE BUMP RELIABILITY FOR FLIP CHIP DEVICE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April \mathcal{L}_6 , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stable 4/26/04

TSMC-01-413C

- U.S. Patent 5,543,253 to Park et al., "Photomask for T-Gate Formation and Process for Fabricating the Same," discusses a dual damascene like Photo process for a T-gate.
- U.S. Patent 6,042,996 to Lin et al., "Method of Fabricating a Dual Damascene Structure," discusses a dual damascene process.

The following four U.S. Patents disclose Bump and UBM processes:

- 1) U.S. Patent 6,232,212 to Degani et al., "Flip Chip Bump Bonding."
- 2) U.S. Patent 6,153,503 to Lin et al., "Continuous Process for Producing Solder Bumps on Electrodes of Semiconductor Chips."
- 3) U.S. Patent 6,130,141 to Degani et al., "Flip Chip Metallization."
- 4) U.S. Patent 6,118,180 to Loo et al., "Semiconductor Die Metal Layout for Flip Chip Packaging."

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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